CLAIMS

1. A method for implementing a logic circuit with integrated logic and latch design, the method comprising the steps of:

providing a clock input to the logic circuit;

providing one or more static signal inputs to the logic circuit;

generating one or more dynamic signal inputs by dynamically gating the one or more static signal inputs with the clock signal;

applying the one or more dynamic signal inputs to the logic circuit;

generating one or more dynamic signal outputs of the logic circuit;

precharging the one or more dynamic signal outputs based on the clock signal;

evaluating the one or more dynamic signal outputs when the one or more dynamic signal outputs are not being precharged;

holding the one or more dynamic signal outputs when the one or more dynamic signal outputs are neither being precharged nor being evaluated; and

converting the one or more dynamic signal outputs into one or more static signal outputs.

2. The method of Claim 1, wherein the one or more static signal inputs comprise complementary static signal inputs.

3. The method of Claim 1, wherein the one or more dynamic signal inputs comprise one or more delayed signal inputs.

4. The method of Claim 1, further comprising the step of applying one or more static signal inputs to the logic circuit.

5. The method of Claim 1, wherein the step of evaluating the one or more dynamic signal outputs follows the step of precharging the one or more dynamic signal outputs.

6. The method of Claim 1, wherein the step of holding the one or more dynamic signal outputs follows the step of evaluating the one or more dynamic signal outputs.

7. An apparatus for implementing a logic circuit with integrated logic and latch design, the method comprising:

means for providing a clock input to the logic circuit;

means for providing one or more static signal inputs to the logic circuit;

means for generating one or more dynamic signal inputs by dynamically gating the one or more static signal inputs with the clock signal;

means for applying the one or more dynamic signal inputs to the logic circuit;

means for generating one or more dynamic signal outputs of the logic circuit;

means for precharging the one or more dynamic signal outputs based on the clock signal;

means for evaluating the one or more dynamic signal outputs when the one or more dynamic signal outputs are not being precharged;

means for holding the one or more dynamic signal outputs when the one or more dynamic signal outputs are neither being precharged nor being evaluated; and

means for converting the one or more dynamic signal outputs into one or more static signal outputs.

8. The apparatus of Claim 7, wherein the one or more static signal inputs comprise complementary static signal inputs.

9. The apparatus of Claim 7, wherein the one or more dynamic signal inputs comprise one or more delayed signal inputs.

10. The apparatus of Claim 7, further comprising means for applying one or more static signal inputs to the logic circuit.

11. A computer program product for implementing a logic circuit with integrated logic and latch design, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer program code for providing a clock input to the logic circuit;

computer program code for providing one or more static signal inputs to the logic circuit;

computer program code for generating one or more dynamic signal inputs by dynamically gating the one or more static signal inputs with the clock signal;

computer program code for applying the one or more dynamic signal inputs to the logic circuit;

computer program code for generating one or more dynamic signal outputs of the logic circuit;

computer program code for precharging the one or more dynamic signal outputs based on the clock signal;

computer program code for evaluating the one or more dynamic signal outputs when the one or more dynamic signal outputs are not being precharged;

computer program code for holding the one or more dynamic signal outputs when the one or more dynamic signal outputs are neither being precharged nor being evaluated; and

computer program code for converting the one or more dynamic signal outputs into one or more static signal outputs.

12. The computer program product of Claim 11, wherein the one or more static signal inputs comprise complementary static signal inputs.

13. The computer program product of Claim 11, wherein the one or more dynamic signal inputs comprise one or more delayed signal inputs.

14. The computer program product of Claim 11, further comprising computer program code for applying one or more static signal inputs to the logic circuit.

15. A logic circuit with integrated logic and latch design comprising:

a clock gating circuit configured for receiving a clock signal and one or more static signal inputs and for generating one or more dynamic signal inputs by dynamically gating the one or more static signal inputs with the clock signal;

an evaluation logic circuit coupled both to the clock gating circuit for receiving the one or more dynamic signal inputs and to a dynamic node for carrying a dynamic signal output of the evaluation logic circuit;

a precharge circuit coupled to the dynamic node for precharging the dynamic node based on the clock signal, the dynamic node being evaluated when the precharge circuit is not precharging the dynamic node;

a keeper circuit coupled to the dynamic node for holding the dynamic signal output when the dynamic node is neither being precharged nor being evaluated; and

a conversion circuit coupled to the dynamic node for converting the dynamic signal output into a static signal output.

16. The logic circuit of Claim 15, wherein the one or more static signal inputs comprise first, second, and third static signal inputs, and wherein the clock gating circuit comprises:

a first AND logic circuit for receiving the clock signal and the first static signal input and for generating a first dynamic signal input;

a first inverter for receiving the first static signal input and for generating a first complement static signal input;

a second AND logic circuit for receiving the clock signal and coupled to the first inverter for receiving the first complement static signal input, the second AND logic circuit generating a first complement dynamic signal input;

a second inverter for receiving the clock signal and for generating an STRB signal;

a third inverter coupled to the second inverter for receiving the STRB signal and for generating a PC signal;

a delay block coupled to the third inverter for receiving the PC signal and for generating a CLKBD signal;

a third AND logic circuit coupled to the delay block for receiving the CLKBD signal and configured for receiving the second static signal input, the third AND logic circuit generating a second dynamic signal input;

a fourth inverter for receiving the second static signal input and for generating a second complement static signal input;

a fourth AND logic circuit for receiving the CLKBD signal and coupled to the fourth inverter for receiving the second complement static signal input, the fourth AND logic circuit generating a second complement dynamic signal input; and

a fifth inverter for receiving the third static signal input and for generating a third complement static signal input.

17. The logic circuit of Claim 16, wherein the precharge circuit comprises an electronic switch coupled between a supply voltage and the dynamic node and coupled to the clock gating circuit for receiving the PC signal, the PC signal controlling the electronic switch.

18. The logic circuit of claim 17, wherein the electronic switch comprises a p-channel metal-oxide-silicon (PMOS) transistor having source, gate, and drain terminals, the source terminal being coupled to the supply voltage, the gate terminal being coupled to the clock gating circuit for receiving the PC signal, and the drain terminal being coupled to the dynamic node.

19. The logic circuit of Claim 16, wherein the keeper circuit comprises:

a sixth inverter coupled to the dynamic node for receiving the dynamic signal output and generating an inverted dynamic signal output;

a first electronic switch coupled between a supply voltage and the dynamic node and coupled to the sixth inverter for receiving the inverted dynamic signal output as a control signal; and

second and third electronic switches coupled in series between the dynamic node and ground, the second electronic switch being coupled to the clock gating circuit for receiving the PC signal as a control signal, and the third electronic switch being coupled to the sixth inverter for receiving the inverted dynamic signal output as a control signal.

20. The logic circuit of Claim 19, wherein the first electronic switch comprises a p-channel metal-oxide-silicon (PMOS) transistor, and wherein the second and third electronic switches each comprise an n-channel metal-oxide-silicon (NMOS) transistor.

21. The logic circuit of Claim 16, wherein the conversion circuit comprises a cross-coupled NAND coupled to the dynamic node for receiving the dynamic signal output and to the clock gating circuit for receiving the CLKBD signal.

22. The logic circuit of Claim 16, wherein the evaluation logic circuit comprises a tree of electronic switches, the tree being coupled between the dynamic node and ground.

23. The logic circuit of Claim 22, wherein the tree comprises top, middle, and bottom portions, wherein the top portion is coupled to the clock gating circuit for receiving the second dynamic signal input and the second complement dynamic signal input, and wherein the bottom portion is coupled to the clock gating circuit for receiving the first dynamic signal input and the first complement dynamic signal input.

24. The logic circuit of Claim 23, wherein the middle portion is coupled to the clock gating circuit for receiving the third static signal input.

25. The logic circuit of Claim 23, wherein the middle portion is coupled to the clock gating circuit for receiving the third complement static signal input.

26. The logic circuit of Claim 23, wherein the middle portion is coupled to the clock gating circuit for receiving both the third static signal input and the third complement static signal input.

27. The logic circuit of Claim 22, wherein the electronic switches each comprise an n-channel metal-oxide-silicon (NMOS) transistor.